

Sub C33
19. (Amended) A semiconductor device as claimed in claim 13 or 14, wherein said circuit comprising the switch elements is a clock circuit or a flip-flop circuit.

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20. (Amended) A semiconductor device as claimed in claim 13 or 14, wherein said switch elements are formed of field effect transistors in said basic cells.

21. (Amended) A semiconductor device as claimed in any one of claims 7 to 14, wherein said basic cells include the p-channel type field effect transistors and n-channel type field effect transistors.

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22. (Amended) A semiconductor device as claimed in any one of claims 7 to 12, wherein a wiring electrically connected to the gate electrode of said switch element is formed of the wiring of the third wiring layer and this wiring is arranged in parallel to said power supply wirings.

92 23. (Amended) A semiconductor device as claimed in any one of claims 7 to 14, wherein a semiconductor region for power feeding to supply the predetermined voltage to the semiconductor region formed in said semiconductor substrate is formed in the region between the internal circuit region where a plurality of said basic cells are arranged and the peripheral circuit region at the external side of said internal circuit region.

Sub C33 93 27. (Amended) A semiconductor device as claimed in any one of claims 1 to 14, wherein said switch elements are turned ON in the normal operation period of semiconductor device and the power supply voltage is applied from said power supply wirings to the semiconductor region formed in said semiconductor substrate and said switch elements are turned OFF in the testing or waiting period of semiconductor device and the voltage different from said power supply voltage is applied to said semiconductor region.

37. (Amended) A semiconductor device as claimed in claim 33,
34 or 35, wherein the wiring connected to the gate
electrode of the field effect transistor forming said
switch element is arranged to surround the internal
circuit region of a semiconductor device.

38. (Amended) A semiconductor device as claimed in any one of
claims 33 to 35 , wherein at least one of a pair of
semiconductor regions for source and drain of the field
effect transistors unused for said input/output
circuits is electrically connected to said power supply
wiring to form a capacitance element.

45. A semiconductor device as claimed in any one of
claims 7 to 12, wherein a logic circuit is
formed using said basic cells and said logic circuit
is formed among the basic cells forming said switch
element.

46. A semiconductor device claimed in claim 9, 11,
or 12 ; wherein a logic circuit is formed using said
basic cells, said unused field effect transistor is the
field effect transistor of basic cell not forming a
logic circuit and said logic circuit and unused basic
cells are formed among the basic cells forming said
switch element.